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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/728,301	12/01/2000	Roubik Gregorian	10262-01400US	4922

7590 01/06/2004

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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2631	4

DATE MAILED: 01/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/728,301	GREGORIAN ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it is too short. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-4, 7-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Shyue U.S. Patent No 6,359,936 B1.

As per claim 1, Shyue teaches a digital line build out circuit comprising: a memory storing a plurality of digitized waveforms (see fgs. 4-6, 8a-8b elements 80 or 100 and col.2, lines 5-6 and col.6, lines 65-67 and col.7, lines 1-20); a selection circuit, coupled to said memory, to select (see figs.4-6, 8a-8b elements 74, 184, 200, 284 and col.9, lines 10-25 and col.10, lines 43-67) certain

ones of said waveforms corresponding to an anticipated amount of signal degradation over a transmission line; and a digital to analog converter (see element 44 and col.7, lines 13-20) to convert said certain ones of said waveforms into analog waveforms for transmission.

As per claim 2, Shyue does include a counter (see fig.4 element 54) having an output coupled to inputs of said memory for sequentiallyselecting multiple samples of said digitized waveforms during a period.

As per claim 3, Shyue does include said memory comprises a ROM (fig.5 element 80).

As per claims 4 and 7, Shyne does include an adder or summer is the same as the claimed (a combining circuit) (see fig.7 element 290 and col.9, lines 37-40), coupled between said memory and said digital to analog converter, to combine a portion of a current digitized waveform with a portion of at least one previous digitized waveform.

As per claim 8, Shyue teaches a digital line build out circuit comprising: a memory storing a plurality of digitized waveforms (see figs. 4-6, 8a-8b elements 80 or 100 and col.2, lines 5-6 and col.6, lines 65-67 and col.7, lines 1-20); a selection circuit, coupled to said memory select (see figs.4-6, 8a-8b elements 74, 184, 200, 284 and col.9, lines 10-25 and col.10, lines 43-67), to select certain ones of said waveforms corresponding to an anticipated amount of signal degradation over a transmission line; a digital to analog converter (see element 44 and col.7, lines 13-20) to convert said certain ones of said waveforms into analog waveforms for transmission; a counter (see figs 4-6, 8a-8b element 54) having an output coupled to inputs of said memory for sequentially selecting multiple samples of said digitized waveforms during a period; an adder or

summer is the same as the claimed (a combining circuit) (see fig.7 element 290 and col.9, lines 37-40), coupled between said memory and said digital to analog converter, to combine a portion of a current digitized waveform with a portion of at least one previous digitized waveform.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-6 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shyue U.S. Patent NO 6,359,936 B1 in view of Sung U.S. Patent No 5,808,688.

As per claim 5, Shyue discloses all the features of the claimed invention except said combining circuit includes at least one delay element for delaying an output of said memory for said previous digitized waveform for combination with said current digitized waveform.

Sung teaches combining circuit includes at least one delay element for delaying (see fig.3a elements D1-D7 and col.4, lines 39-67) an output of said memory for said previous digitized waveform for combination with said current digitized waveform.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Sung into Shyue as to perform interpolation in order to provide a high quality picture during format conversion as taught by Sung (see col.2, lines 5-7)

As per claim 6, Sung teaches delay element delays a data bit, and further comprising a multipliers is considered as the claimed (circuit for gating) (see fig. 3a elements 361-372 and col.4, lines 47-67) a portion of said digitized waveform from said memory based on a value of said data bit. Therefore implementing the teaching of Sung into Shyue would have been obvious to one skilled in the art as to perform interpolation in order to provide a high quality picture during format conversion as taught by Sung (see col.2, lines 5-7).

As per claim 9, Shyue teaches a digital line build out circuit comprising: a memory storing a plurality of digitized waveforms (see figs. 4-6, 8a-8b elements 80 or 100 and col.2, lines 5-6 and col.6, lines 65-67 and col.7, lines 1-20) corresponding to different anticipated amounts of signal degradation over a transmission line, each of said digitized waveforms having a plurality of separately addressable portions; a an adder or summer is the same as the claimed (a combining circuit) (see fig.7 element 290 and col.9, lines 37-40) having inputs coupled to outputs of switching circuits (see fig.7 element 288) for combining multiple ones of said separately addressable portions; a digital to analog converter (see element 44 and col.7, lines 13-20) coupled to an output of said combining circuit; a shift register is the same as the claimed (configuration input) (see fig.6 element 58 and col.9, lines 3-5), coupled to said memory, for selecting a desired one of said plurality of digitized waveforms; and a counter (see figs 4-6, 8a-8b element 54), coupled to said memory, for sequentially selecting a plurality of digitized values for said separately addressable portions.

However Shyue does not teach a data line coupled to a plurality of serial delay elements; a plurality of gating circuits having a first input coupled to one of said data line and an output of each of said delay elements, and a second input coupled to an output of said memory for one of said separately addressable portions; a combining circuit having inputs coupled to outputs of said gating circuits for combining multiple ones of said separately addressable portions.

Sung teaches a data line coupled a plurality of serial delay elements (see fig.3a elements D1-D7 and col.4, lines 39-67); a plurality of multipliers is considered as the claimed (gating circuits) (see fig.3a elements 361-373 and col.4, lines 46-67) having a first input coupled to one of said data line and an output of each of said delay elements, and a second input coupled to an output of said memory (see fig.3a element 35) for one of said separately addressable portions; a an adder or summer is the same as the claimed (a combining circuit) (see fig.3a elements 365, 375 and col.4, lines 49-67 and col.9, lines 37-40) having inputs coupled to outputs of said gating circuits for combining multiple ones of said separately addressable portions.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Sung into Shyue as to perform interpolation in order to provide a high quality picture during format conversion as taught by Sung (see col.2, lines 5-7)

As per claims 10 and 11, Shyne does teach said memory is a ROM (see fig.5 element 80) having a plurality of memories.

As per claim 12, Sung teaches a multiplier circuits. Therefore inplementing the teaching of Sung into Shyne would have been obvious to one skilled in the art as to perform interpolation in

order to provide a high quality picture during format conversion as taught by Sung (see col.2, lines 5-7).

As per claim 13 Shyue does teach a selector circuits (see fig.8b element 284).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lyon U.S. Patent No 5,602,762 teaches a digital sample rate conversion.

Sung et al U.S. Patent No 6,385,259 B1 teaches a composite code match filters.

Marguinaud et al U.S. Patent No 5,886,913 teaches a method of synthesizing a finite response.

Okamura et al U.S. Patent No 5,559,962 teaches a data transmission system.

Lee et al U.S. Patent No 6,138,132 teaches a high speed ROM based nyquist filter.

Thomas U.S. Patent No 6,487,242 B1 teaches a method an apparatus for VCO modulation.

Matui U.S Patent No 5,942,955 teaches a Quasi GMSK.

Patire U.S. Patent No 6,430,232 B1 teaches a phase constellation modulator.

Furukawa et al U.S. Patent No 6,272,509 B1 teaches a filter device.

Hilton et al U.S. patent No 6,185,594 B1 teaches a versatile signal generator.

Sagawa U.S. Patent No 5,796,782 teaches a digital modulator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is (703) 308-9573. The

examiner can normally be reached on Monday-Thursday from 8:00 AM - 5:30 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour , can be reached on (703) 306-3034. The fax phone number for this Group is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Emmanuel Bayard

Primary Examiner

December 31, 2003